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AREA OPTIMIZED CARDINAL MULTI WAVELETS FOR WIRELESS COMMUNICATION

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ABSTRACT

New technologies are emerging to take the challenges in the wireless communication. According to the requirements for the next generation technologies have led to unparalleled insist for high speed architectures for complex signal processing applications. In this paper DMWT and IDMWT is implemented on FPGA optimizing area, speed and power. The model is tested for its functionality using HDL code and is synthesized using Xilinx ISE targeting FPGA. The DMWT-OFDM achieves higher BER performances compared with DWT-OFDM and FFT-OFDM. The modified DMWT architecture operates at 300MHz frequency and occupies area of less than 1%, with power consumption less than 25mW. The proposed design is suitable for real time and low power applications

Keywords— OFDM, DMWT, IDMWT, FPGA

1. INTRODUCTION

The key driving forces for the continued technology evolution in wireless communications are the high data rates and high spectral efficiency. To further improve the data rate and the system performance, several advancements have been introduced. Orthogonal Frequency division multiplexing (OFDM) provides an efficient means to handle high-speed data streams over a multipath fading environment. It is a technique of transmitting data by dividing the input data stream into parallel sub-streams that are each modulated and multiplexed onto the channel at different carrier frequencies.

The fundamental principle of the OFDM system is to decompose the high rate data stream into N parallel lower rate data streams or channels, one for each subcarrier. Each sub-carrier is modulated at a low symbol rate with a conventional modulation Scheme, maintaining total data rates similar to conventional single-carrier modulation schemes in the same bandwidth. A sufficiently high value of N makes the individual bandwidth (W/N) of subcarriers narrower than the coherence bandwidth of the channel.

The advantage of OFDM over single carrier schemes is its ability to manage with ruthless channel conditions without use of complex equalization filters. Channel equalization is simplified because OFDM may be viewed as using many slowly-modulated narrowband signals rather than one promptly modulated wideband signal. The choice of entity subcarriers is such that they are orthogonal to each other, which allows for the overlapping of subcarriers because the orthogonality ensures the separation of subcarriers at the receiver end. This approach results in a better spectral efficiency than other types of systems like Frequency Division Multiple Access, where no spectral overlap of carriers is allowed. The major involvement to the OFDM execution was the application of the Fast Fourier Transform (FFT) to the modulation and demodulation processes. FFT has a major disadvantage arising from using rectangular window, which creates side lobes.

Moreover, the pulse shaping function used to modulate each subcarrier extends to infinity in the frequency domain. This leads to high interference and lower performance levels. Inter carrier interference (ICI) and inter symbol interference (ISI) can be avoided by adding a cyclic prefix (CP) to the head of OFDM symbol. But, this reduces the spectrum efficiency. Another major problem of FFT based OFDM system is the high peak to average power ratio (PAPR). Due to this problem other type of modulation scheme based on DWT to generate the carrier is adopted. Many authors have proposed DWT for OFDM, DWT-OFDM has a high degree of side lobe suppression and the loss of orthogonality leads to lesser inter symbol interference (ISI) and inter carrier interference (ICI) than in conventional OFDM system. By using the transform, the spectral containment of the channels is better since it does not use CP. One type of wavelet transform is namely as Discrete Wavelet Transform OFDM (DWT-OFDM). Further performance gains can be made by looking into alternative orthogonal basis functions and finding a better transform rather than Fourier and wavelet transform. Multiwavelet is a new concept has been proposed in recent years. Multiwavelets have several advantages compared to single wavelets.

A single wavelet cannot simultaneously possess all the properties of orthogonality, symmetry, short support, and vanishing moments. Multiwavelets are very similar to wavelets but have some important differences. In particular, whereas wavelets have an associated scaling function and wavelet function, multiwavelets have two or more scaling and wavelet functions. For all the priorities of multiwavelet, a natural thought is applying it on OFDM. the DMWT based OFDM achieves BER 10-4 at 11.5 dB, In this paper, FPGA implementation of DMWT based OFDM is carried out optimizing area and power. Section II discusses Multiwavelet based OFDM, section III discusses design of DMWT architecture, Section IV results and discussion and section V presents conclusion.

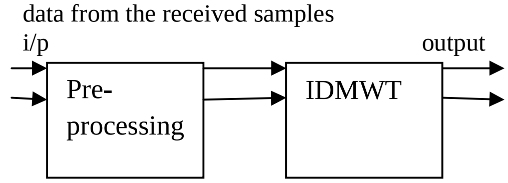
2. MULTIWAVELET BASED OFDM

Alternative option to the wavelet transform is the multiwavelet transform. Multiwavelets are very similar to scalar wavelets but have some important differences. In particular, whereas wavelets have an associated scaling function $\Phi(t)$ and wavelet function $\Psi(t)$, multiwavelets have two or more scaling and wavelet functions. For notational convenience, the set of scaling functions can be written using the vector notation $\Phi(t)=[\phi_1(t)\ \ \phi_2(t)\ \ \cdots\ \ \phi_r(t)]^T$, where $\Psi(t)$ is called the multiscaling function. Likewise, the multiwavelet function is defined from the set of wavelet functions as $\Psi(t)=[\psi_1(t)\ \ \psi_2(t)\ \ \cdots\ \ \psi_r(t)]^T$. When r=1, $\Psi(t)$, is called a scalar wavelet, or simply wavelet. While in principle can be arbitrarily large, the multiwavelets studied to date are primarily for r=2. The multiwavelet two-scale equations resemble those for scalar wavelets.

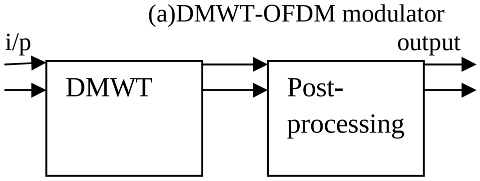
$$\Phi(2^j t) = \sum_k H_{j+1}(k)\Phi(2^{j+1}t-k)$$

$$\Psi(2^j t) = \sum_k G_{j+1}(k)\Phi(2^{j+1}t-k)$$

Note, however, that H_k and G_k are *matrix* filters, i.e., H_k and G_k are matrices for each integer . The matrix elements in these filters provide more degrees of freedom than a traditional scalar wavelet. These extra degrees of freedom can be used to incorporate useful properties into the multiwavelet filters, such as orthogonality, symmetry and high order of approximation. The key, then, is to figure out how to make the best use of these extra degrees of freedom. Multifilter construction methods are already being developed to exploit them. Multiwavelet based OFDM architecture is shown in figure below. Input data is converted into parallel data before IDWT processing is performed. For OFDM there are very few multiwavelets reported. A very important Multiwavelets filteris the cardibal2 filter. In cardibal2 multiwavelets setting, multiscaling and Multiwavelets functions coefficients are 2X2 matrices and during transformation step they must multiply vectors (instead of scalars). This means that multifilter bank need two input rows. The aim of preprocessing is to associate the given scalar input signal of length N to a sequence of length-two vectors in order to start the analysis algorithm and to reduce the noise effects. In the one dimensional signals the “repeated row” scheme is convenient and powerful to implement. The OFDM modulator and demodulator of DMWT-based OFDM are shown in figure1. The input data is preprocessed and is modulated using Inverse DMWT (IDWMT). In the preprocessing state the input samples are symmetrically extended to the size of the IDMWT coefficients for modulation. At the receiver, DMWT demodulation is performed on the received signals and the post processing logic retrieves the modulated data from the received samples



(a)DMWT-OFDM modulator



(b)DMWT-OFDM modulator

Figure. 1 DMWT-OFDM modem system

Then the computation of IDMWT for 1-D signal is achieved by using an over-sampled scheme of pre-processing (repeated row), the Inverse Discrete Multiwavelets Transform (IDMWT) matrix is doubled in dimension compared with that of the input, which should be a square matrix N x N where N must be power of 2. Transformation matrix dimensions are equal to input signal dimensions after pre-processing. To compute a single-level 1-D discrete multiwavelets transform, the next steps should be followed:

1. Checking input dimensions: input vector should be of length N, where N must be power of 2.
2. Constructing a transformation matrix, *W*, using cardibal low and high pass filters matrices given in equations. After substitution cardibal matrix filter coefficients values, a 2N X 2N transformation matrix results.

Cardinal multiwavelets are called balanced multiwavelets, were introduced to avoid the prefiltering step in multiwavelet computations Multiwavelet bases, for which the zero moment properties carry over to the discrete-time filter bank. We were obtained a four-balanced cardinal orthogonal multiwavelet system with filters of length 23. The cardbal4 filter co-efficient of cardinal multiwavelet is,

$$H0 = \begin{bmatrix} 0 & 0 \\ 1 & 0 \end{bmatrix} \quad H1 = \begin{bmatrix} 0.173 & 1/\sqrt{2} \\ 0.662 & 0 \end{bmatrix}$$

$$H2 = \begin{bmatrix} 0.937 & 0 \\ -0.24 & 1 \end{bmatrix} \quad H3 = \begin{bmatrix} 0.242 & 0 \\ 0.031 & 0 \end{bmatrix} \quad (1)$$

$$H4 = \begin{bmatrix} 0.031 & 0 \\ -0.24 & 0 \end{bmatrix} \quad H5 = \begin{bmatrix} 1 & 0 \\ 0.022 & 0 \end{bmatrix}$$

$$G0 = \begin{bmatrix} -0.02 & 0 \\ 1 & 0 \end{bmatrix} \quad G1 = \begin{bmatrix} -0.17 & 1/\sqrt{2} \\ -0.66 & 0 \end{bmatrix}$$

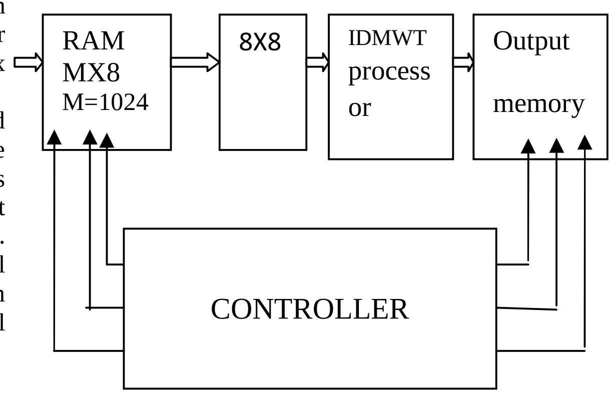
$$G2 = \begin{bmatrix} -0.93 & 0 \\ 0.242 & 1 \end{bmatrix} \quad G3 = \begin{bmatrix} -0.24 & 0 \\ -0.03 & 0 \end{bmatrix} \quad (2)$$

$$G4 = \begin{bmatrix} -0.03 & 0 \\ 0.246 & 0 \end{bmatrix} \quad G5 = \begin{bmatrix} -1 & 0 \\ -0.02 & 0 \end{bmatrix}$$

$$\begin{bmatrix} H_0 & H_1 & H_2 & H_3 & 0 & 0 & \cdots & 0 & 0 & 0 & 0 \\ 0 & 0 & H_0 & H_1 & H_2 & H_3 & \cdots & 0 & 0 & 0 & 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ H_2 & H_3 & 0 & 0 & 0 & 0 & \cdots & 0 & 0 & H_0 & H_1 \\ G_0 & G_1 & G_2 & G_3 & 0 & 0 & \cdots & 0 & 0 & 0 & 0 \\ 0 & 0 & G_0 & G_1 & G_2 & G_3 & \cdots & 0 & 0 & 0 & 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \cdots & \vdots & \vdots & \vdots & \vdots \\ 0 & 0 & 0 & 0 & 0 & 0 & \cdots & G_0 & G_1 & G_2 & G_3 \\ G_2 & G_3 & 0 & 0 & 0 & 0 & \cdots & 0 & 0 & G_0 & G_1 \end{bmatrix} \quad (3)$$

3. Pre-processing the input signal by repeating the input stream with the same stream multiplied by a constant $1/\sqrt{2}$.
4. Transformations of input vector which can be done by applying matrix multiplication to the 2Nx2N constructed transformation matrix by the 2Nx1 pre-processing input vector.

3. DESIGN OF DMWT/IDMWT ARCHITECTURE



The DMWT-OFDM achieves higher BER performances compared with DWT-OFDM and FFT-OFDM. However, the number of coefficients required to compute forward and inverse DMWT are 2(2Nx2N), where N is the size of input samples. In order to compute DMWT it is required to perform large number of multiplications and additions. Thus it is required to reduce the computation complexity of DMWT computation to enhance speed, area and Power performances of DMWT-OFDM compared with DWT-OFDM.

The transformation matrix based on cardibal filters for DMWT is chosen to be of size 8 x 8. This is the minimum size for cardibal based filters; higher orders would lead to complexity in hardware. The input is taken into group of 6 samples, and is repeated with scaled values. The input matrix which is of size 6 x 1 is resized to 12 x 1 after extension and scaling as shown in equation 4.

The input matrix is transformed to output using the cardibal filter. After matrix multiplication we get equations for computing the output matrix of size 12 x 1. From the equations, there are redundant factors between samples y0 andy11, in order to eliminate redundancies and reduce computation time; the equations are regrouped by reducing the common factors. The simplified constants are scaled by 128 to convert the fractions to nearest integers. Due to rounding effect the loss is restricted to less than 2%. The simplified expression for cardbal filters are rewritten in matrix form, from the two matrices it is found that the input samples are of size 6x1 and are used simultaneously to compute the output samples y0 to y11. Here it is scaled with scaling factor 128. The table below shows co-efficient before and after scaling.

Table1: Scaled and Un scaled co-efficient

Before scaling	After scaling
0.171	21
0.195	25
0.707	90
1.644	210
1.022	130
0.488	62
0.242	30
0.153	19
-0.226	-28
0.7382	94
-1.43	-184
0.997	125
0.675	86
-1.63	-213

Y0 = 21*x0+25*x2+90*x3+210*x4 (4)
Y1 = 130*x0+62*x2-28*x4+128*x5 (5)
Y2 = 210*x0+30*x2+19*x4+90*x5 (6)
Y3 = -28*x0+128*x1+94*x3 28*x4 (7)
Y4 = 30*x0 +19*x2+64*x3 212*x4 (8)
Y5 = 94*x0+28*x2-19*x4+ 90*x5 (9)
Y6 = 24*x0-25*x2+90*x3-184*x4 (10)
Y7 = 125*x0-62*x2+28*x4+128*x5 (11)
Y8 = -210*x0-32*x2-19*x4+212*x4 (12)
Y9 = 28*x0+128*x1+86*x2-28*x4 (13)
Y10 = -19*x0+64*x1-213*x2-24*x4 (14)
Y11= -28*x0+19*x2+90*x3+125*x4 (15)

The filter coefficients are obtained from the simplified equations. Reducing the above equations into matrix form. The simplified equations derived from above matrix are used in design of multiwavelet architecture. The optimized architecture consists of a FIFO of size 4, that stores the input samples, and the FIFO are accessed to compute the output samples as per the simplified equations. The optimized architecture is modelled using HDL and is simulated using ModelSim. In this work a cardbal based DMWT and IDMWT is implemented on FPGA optimizing area, power and speed performances.

4. RESULTS AND DISCUSSION

In this section, VLSI implementation of DMWT for OFDM is presented. The modeled HDL is simulated and tested for its functionality; the functionally verified HDL code is synthesized using Xilinx ISE targeting Virtex-5 FPGA. The design consists of 110 million gates and has 1136 I/Os. The synthesized net list and synthesis report are analyzed for the performance of designed DMWT architecture. The results obtained are compared and discussed in this section.

Table2: Device Utilization

Logic Utilization	Used	Avail able	Utiliza tion
Number of sliced LUTs	1	63,400	1%
Number of bonded IOB’S	15	210	7%
IOB Flip Flops	64		
Number of DSP48E1s	31	240	13%

Target Device: xc2vp30-7-ff896
Minimum input arrival time before clock: 8.362ns
Maximum output required time after clock: 3.293ns
Total memory usage is 144660 kilobytes

From the optimized architecture the number of multipliers and adders are minimized. Apart from reduction in multipliers and adders, it is also found that the throughput and latency of the optimized design is also improved. The arithmetic unit designed works on fixed point number system and thus introduces loss when compared with floating point number system. The DMWT architecture operates at a maximum frequency of 340MHz and consumes power less than 25mW. The power consumption is reduced by adopting various low power techniques as recommended for FPGA implementation.

5. CONCLUSION

In this work, we propose a modified DMWT architecture based on cardbal filter. The DMWT coefficients that are fractions are converted to integers and are modified to reduce the number of multiplications and additions. The reduced cardbal filter coefficients are used to process the data, thus reducing the computation complexity and making it suitable for FPGA implementation. The modified equations are modeled using HDL and implemented on FPGA. The design operates at maximum frequency of 300MHz and consumes less than 1% resources and thus is suitable for real time applications.

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